**Index Number – 210098R**

**Name – De Silva A.P.C.**

**Assigned Task –**

Understanding the concepts and then designing & developing a 2 to 4 decoder.

Then Designing and developing a 3 to 8 decoder using 2 to 4 decoders.

After that, designing and developing 8 to 1 multiplexer using a 3 to 8 decoder after properly identifying the relevant logic circuit.

(Verification of the specific functionalities through simulations is included in each one of them.)

**VHDL codes –**

***Decoder\_2\_to\_4.vhd***

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-- Company:

-- Engineer:

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-- Create Date: 03/21/2023 09:43:25 PM

-- Design Name:

-- Module Name: Decoder\_2\_to\_4 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Decoder\_2\_to\_4 is

Port ( I : in STD\_LOGIC\_VECTOR (1 downto 0);

EN : in STD\_LOGIC;

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

end Decoder\_2\_to\_4;

architecture Behavioral of Decoder\_2\_to\_4 is

begin

Y(0)<= not I(0)and not I(1)and EN;

Y(1)<= not I(1)and I(0)and EN;

Y(2)<= I(1)and not I(0)and EN;

Y(3)<= I(0)and I(1)and EN;

end Behavioral;

***TB\_Decoder\_2\_to\_4.vhd***

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-- Company:

-- Engineer:

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-- Create Date: 03/22/2023 12:10:51 AM

-- Design Name:

-- Module Name: TB\_Decoder\_2\_to\_4 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity TB\_Decoder\_2\_to\_4 is

-- Port ( );

end TB\_Decoder\_2\_to\_4;

architecture Behavioral of TB\_Decoder\_2\_to\_4 is

COMPONENT Decoder\_2\_to\_4

PORT( I : in STD\_LOGIC\_VECTOR (1 downto 0);

EN : in STD\_LOGIC;

Y : out STD\_LOGIC\_VECTOR (3 downto 0));

END COMPONENT;

signal I0,I1 : STD\_LOGIC ;

signal Y0,Y1,Y2,Y3 : STD\_LOGIC ;

signal EN : STD\_LOGIC;

begin

UUT: Decoder\_2\_to\_4 PORT MAP(

I(0) => I0,

I(1) => I1,

Y(0) => Y0,

Y(1) => Y1,

Y(2) => Y2,

Y(3) => Y3,

EN => EN);

process

begin

EN <='0';

I0 <= '0';

I1 <= '0';

WAIT FOR 100 ns;

I0 <= '1';

WAIT FOR 100 ns;

I0 <= '0';

I1 <= '1';

WAIT FOR 100 ns;

I0 <= '1';

WAIT FOR 100 ns;

I0 <= '0';

I1 <= '0';

EN <= '1';

WAIT FOR 100 ns;

I0 <= '1';

WAIT FOR 100 ns;

I0 <= '0';

I1 <= '1';

WAIT FOR 100 ns;

I0 <= '1';

WAIT;

end process;

end Behavioral;

***Decoder\_3\_to\_8.vhd***

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-- Company:

-- Engineer:

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-- Create Date: 03/22/2023 02:58:34 AM

-- Design Name:

-- Module Name: Decoder\_3\_to\_8 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Decoder\_3\_to\_8 is

Port ( I : in STD\_LOGIC\_VECTOR (2 downto 0);

EN : in STD\_LOGIC;

Y : out STD\_LOGIC\_VECTOR (7 downto 0));

end Decoder\_3\_to\_8;

architecture Behavioral of Decoder\_3\_to\_8 is

component Decoder\_2\_to\_4

port(

I: in STD\_LOGIC\_VECTOR;

EN: in STD\_LOGIC;

Y: out STD\_LOGIC\_VECTOR );

end component;

signal I0,I1 : STD\_LOGIC\_VECTOR (1 downto 0);

signal Y0,Y1 : STD\_LOGIC\_VECTOR (3 downto 0);

signal en0,en1, I2 : STD\_LOGIC;

begin

Decode\_2\_to\_4\_0 : Decoder\_2\_to\_4

port map(

I => I0,

EN => en0,

Y => Y0 );

Decode\_2\_to\_4\_1 : Decoder\_2\_to\_4

port map(

I => I1,

EN => en1,

Y => Y1 );

en0 <= NOT(I(2)) AND EN;

en1 <= I(2) AND EN;

I0 <= I(1 downto 0);

I1 <= I(1 downto 0);

I2 <= I(2);

Y(3 downto 0) <= Y0;

Y(7 downto 4) <= Y1;

end Behavioral;

***TB\_Decoder\_3\_to\_8.vhd***

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-- Company:

-- Engineer:

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-- Create Date: 03/22/2023 03:00:12 AM

-- Design Name:

-- Module Name: TB\_Decoder\_3\_to\_8 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity TB\_Decoder\_3\_to\_8 is

-- Port ( );

end TB\_Decoder\_3\_to\_8;

architecture Behavioral of TB\_Decoder\_3\_to\_8 is

COMPONENT Decoder\_3\_to\_8

PORT( I : in STD\_LOGIC\_VECTOR (2 downto 0);

EN : in STD\_LOGIC;

Y : out STD\_LOGIC\_VECTOR (7 downto 0));

END COMPONENT;

signal I0,I1,I2 : STD\_LOGIC ;

signal Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7 : STD\_LOGIC ;

signal EN : STD\_LOGIC;

begin

UUT: Decoder\_3\_to\_8 PORT MAP(

I(0) => I0,

I(1) => I1,

I(2) => I2,

Y(0) => Y0,

Y(1) => Y1,

Y(2) => Y2,

Y(3) => Y3,

Y(4) => Y4,

Y(5) => Y5,

Y(6) => Y6,

Y(7) => Y7,

EN => EN);

process

begin

EN <='0';

I0 <= '0';

I1 <= '1';

I2 <= '0';

WAIT FOR 100 ns;

I2 <= '1';

WAIT FOR 100 ns;

I0 <= '1';

I2 <= '0';

WAIT FOR 100 ns;

EN <='1';

I0 <= '0';

I2 <= '0';

WAIT FOR 100 ns;

I2 <= '1';

WAIT FOR 100 ns;

I0 <= '1';

I2 <= '0';

WAIT FOR 100 ns;

I0 <= '1';

I1 <= '0';

I2 <= '1';

WAIT;

end process;

end Behavioral;

***Mux\_8\_to\_1.vhd***

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-- Company:

-- Engineer:

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-- Create Date: 03/22/2023 01:32:17 PM

-- Design Name:

-- Module Name: Mux\_8\_to\_1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Mux\_8\_to\_1 is

Port ( S : in STD\_LOGIC\_VECTOR (2 downto 0);

D : in STD\_LOGIC\_VECTOR (7 downto 0);

EN : in STD\_LOGIC;

Y : out STD\_LOGIC);

end Mux\_8\_to\_1;

architecture Behavioral of Mux\_8\_to\_1 is

component Decoder\_3\_to\_8

port(

I: in STD\_LOGIC\_VECTOR;

EN: in STD\_LOGIC;

Y: out STD\_LOGIC\_VECTOR );

end component;

signal Decoder\_in : STD\_LOGIC\_VECTOR(7 downto 0);

begin

Decode\_3\_to\_8\_0 : Decoder\_3\_to\_8

port map(

I => S,

EN =>EN,

Y=> Decoder\_in

);

Y <= (D(0) and Decoder\_in(0)) or

(D(1) and Decoder\_in(1)) or

(D(2) and Decoder\_in(2)) or

(D(3) and Decoder\_in(3)) or

(D(4) and Decoder\_in(4)) or

(D(5) and Decoder\_in(5)) or

(D(6) and Decoder\_in(6)) or

(D(7) and Decoder\_in(7));

end Behavioral;

***TB\_Mux\_8\_to\_1.vhd***

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-- Company:

-- Engineer:

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-- Create Date: 03/22/2023 02:21:05 PM

-- Design Name:

-- Module Name: TB\_Mux\_8\_to\_1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity TB\_Mux\_8\_to\_1 is

-- Port ( );

end TB\_Mux\_8\_to\_1;

architecture Behavioral of TB\_Mux\_8\_to\_1 is

COMPONENT Mux\_8\_to\_1

PORT( S : in STD\_LOGIC\_VECTOR (2 downto 0);

D : in STD\_LOGIC\_VECTOR (7 downto 0);

EN : in STD\_LOGIC;

Y : out STD\_LOGIC);

END COMPONENT;

signal S0,S1,S2 : STD\_LOGIC ;

signal D0,D1,D2,D3,D4,D5,D6,D7 : STD\_LOGIC ;

signal EN,Y : STD\_LOGIC;

begin

UUT: Mux\_8\_to\_1 PORT MAP(

S(0) => S0,

S(1) => S1,

S(2) => S2,

D(0) => D0,

D(1) => D1,

D(2) => D2,

D(3) => D3,

D(4) => D4,

D(5) => D5,

D(6) => D6,

D(7) => D7,

Y=>Y,

EN => EN);

process

begin

EN <='0';

S0 <= '0';

S1 <= '1';

S2 <= '0';

D0 <= '0';

D1 <= '1';

D2 <= '0';

D3 <= '0';

D4 <= '1';

D5 <= '1';

D6 <= '1';

D7 <= '1';

WAIT FOR 100 ns;

S2 <= '1';

WAIT FOR 100 ns;

S0 <= '1';

S2 <= '0';

WAIT FOR 100 ns;

EN <='1';

S0 <= '0';

WAIT FOR 100 ns;

S2 <= '1';

WAIT FOR 100 ns;

S0 <= '1';

S2 <= '0';

WAIT FOR 100 ns;

S0 <= '0';

D2 <= '1';

D3 <= '1';

D6 <= '0';

D7 <= '0';

WAIT FOR 100 ns;

S2 <= '1';

WAIT FOR 100 ns;

S0 <= '1';

S2 <= '0';

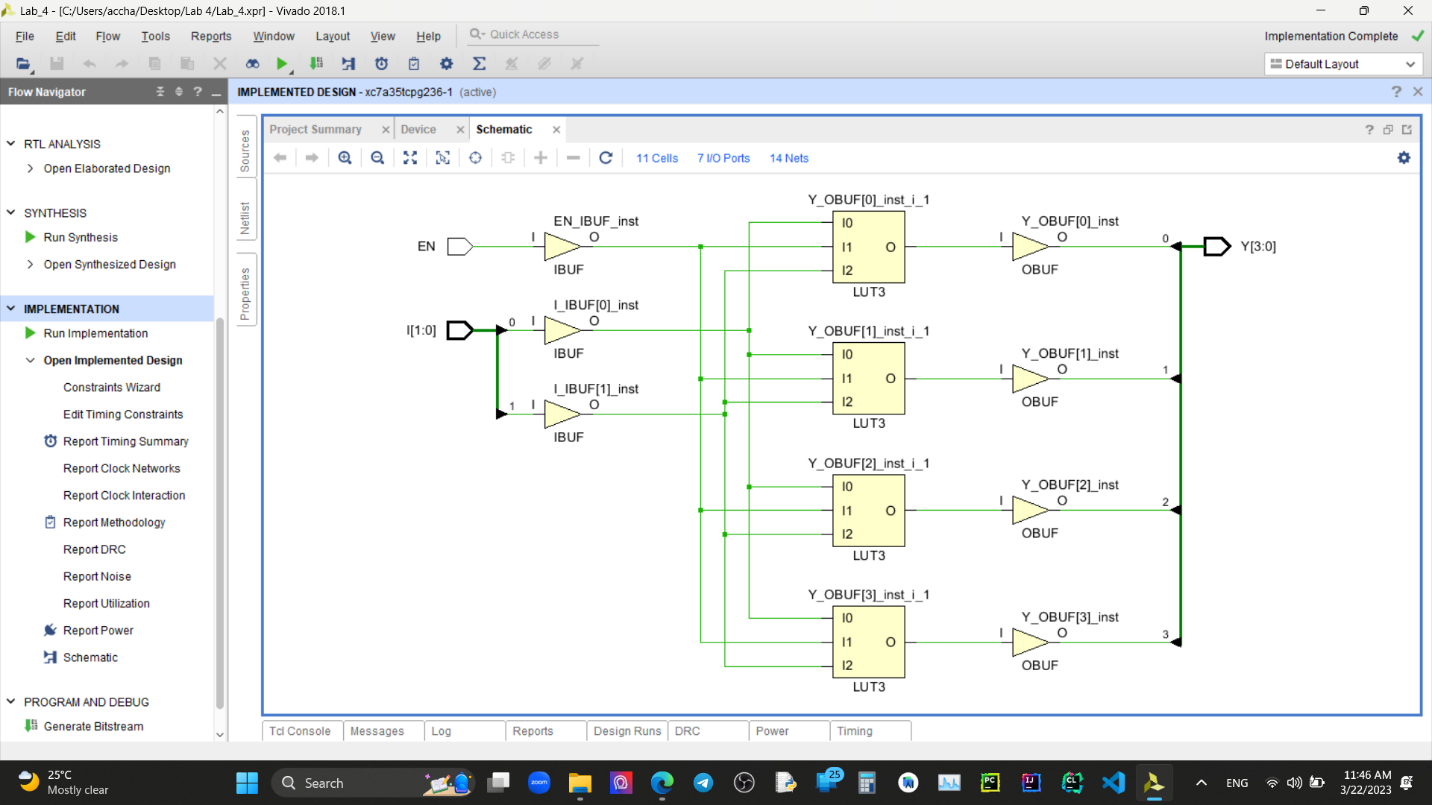
WAIT;

end process;

end Behavioral;

**Design Schematics –**

***2 to 4 Decoder –***

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***3 to 8 Decoder –***

***Diagram

Description automatically generated with medium confidence***

***8 to 1 Multiplexer –***

***A picture containing diagram

Description automatically generated***

**Timing diagrams –**

***2 to 4 Decoder –***

**A screenshot of a computer

Description automatically generated**

***3 to 8 Decoder –***

A screenshot of a computer

Description automatically generated

***8 to 1 Multiplexer –***

A screenshot of a computer

Description automatically generated

(First En was set to 0 for first 300 ns to check its functionality. Then It was set to 1. In first 600ns, D7 to D0 has values 1 1 1 1 0 0 1 0 respectively and then for the sake of accuracy more tests were done by setting D7 to D0 to values 0 0 1 1 1 1 1 0 . The values of S0-S2 is in the way instructed.)

Conclusion **–**

Designing a 2 to 4 decoder, then using that decoder to develop a 3 to 8 decoder, and then using the 3 to 8 decoder to design an 8 to 1 multiplexer is a great exercise in comprehending the hierarchical design process in digital logic.

We can create specific components of the circuit that can be reused in larger designs by dividing a complex problem into smaller, more manageable subproblems. This strategy makes it simpler and easier to test and debug the designs while also reducing the complexity of the overall design.